a charge donor layer comprised of a first Group III-V material; [and]

a channel layer disposed adjacent said charge donor layer and comprised of a second Group III-V material having a bandgap energy lower than the bandgap energy of said first Group III-V material;

a pair of ohmic contacts disposed over first portions of said charge donor and channel layers and a Schottky barrier contact disposed over second portions of said charge donor and channel layers; and

means for shielding at least one of said charge donor and channel layers from the effects of surface charges which are present in regions between gate and drain electrodes of the [transistor.] transistor, said means further comprising:

a first charge screen layer corresponding to a portion of said charge donor layer; and

a second charge screen layer comprised of a third Group III-V material having a bandgap energy lower than the bandgap energy of said first Group III-V material disposed adjacent said gate electrode and at least one drain and source electrodes of said transistor.

2. (~~Amended~~) The [structure,] transistor, as recited in claim 1, wherein [said shielding means includes a portion of] said charge donor layer has [with] a first portion

adjacent said channel being of an undoped Group III-V material, an intermediate [a immediate] portion adjacent said undoped portion comprised of a dopant sheet of N-type dopant having a concentration of dopant atoms confined to a few atomic layer thicknesses of the charge donor layer and a third portion of said layer being a relatively lightly doped region of said charge donor layer with said third portion corresponding to the first charge screen layer.

3. (Amended) The transistor, as recited in claim 2, [1,] wherein said second [shielding means comprises a pair of] charge screen layer [layers] comprised of relatively lightly doped Group III-V material has a dopant concentration of $1X10^{17}$ to $5X10^{17}$ atoms/cc in a region thereof [materials] disposed adjacent the gate electrode, and source and drain electrodes of the [high electron mobility] transistor.

4. (Amended) The [high electron mobility] transistor, as recited in claim 3, wherein said [shielding means further comprises a recess having a first width disposed through the] first charge screen layer has a first recess having a first width disposed therethrough and a second recess aligned over the first recess having a second, substantially larger width than that of the first recess disposed through

a portion of the thickness of the [first charge screen layer and the] second charge screen layer.

13. (Amended) A high electron mobility transistor comprises:

a semi-insulating substrate;

a channel layer comprised of a first Group III-V material disposed over said semi-insulating substrate;

a charge donor layer disposed over said channel layer and [region] comprised of a second Group III-V material having a bandgap higher than that of the corresponding bandgap of the material of the channel layer, a first region of said second [undoped] Group III-V material being undoped, [having a bandgap higher than the corresponding bandgap of the channel layer,] a second region of said charge donor layer having a dopant [profile] confined to a few angstroms thickness of said charge donor layer and having a dopant concentration generally in the range of about $2.0X10^{12}$ to $5X10^{12}$ atoms per square centimeter, [said charge donor layer having] and a third region comprised of a relatively lightly doped portion of said second Group III-V material;

a charge screen layer comprised of a lightly doped N-type region of ~~a second~~ first [the first] Group III-V material disposed over said third region of said charge donor layer;

a pair of spaced contact regions comprised of said ~~second~~ [first] Group III-V material having a dopant concentration greater than about $1X10^{18}$ [a/cc] atoms per cubic centimeter disposed over said charge screen layer;

a gate electrode disposed in Schottky barrier contact with said third ~~portion~~ of said charge donor layer; and

a pair of source and drain electrodes disposed in ohmic contact with said spaced contact ~~layers~~.

~~6~~. (Amended) The transistor, [structure,] as recited in Claim ~~5~~, wherein [said gate electrode is disposed within a first aperture provided in] said third ~~portion~~ of said charge donor layer and a selective portion of said charge screen layer has a first aperture and wherein said charge screen layer and spaced contact ~~layers~~ [layer] have therein a second relatively wide aperture compared to that of the first aperture and said second aperture disposed in alignment over the first aperture and said gate is disposed in said first aperture.

Please add the following Claims 7-16.

~~7~~. The transistor, as recited in Claim 1, wherein said charge donor layer is comprised of aluminum gallium arsenide and said channel layer is comprised of gallium arsenide.

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8. The structure, as recited in claim 1, wherein said first material is aluminum gallium arsenide, said second material is indium gallium arsenide, and said third material is gallium arsenide.

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9. The transistor, as recited in claim 1, wherein said charge donor layer is a first charge donor layer and said transistor further comprises a second charge donor layer comprised of said first Group III-V material disposed on an opposing surface of said channel layer such that said first charge donor layer and said second charge donor layer are disposed to sandwich said channel layer.

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10. The transistor, as recited in claim 9, wherein said second charge donor layer comprises:

a first portion adjacent said channel layer being of an undoped first Group III-V material, an intermediate portion of said charge donor layer adjacent said undoped portion comprised of a dopant sheet of n-type dopant having a concentration of dopant atoms confined to a few atomic layer thicknesses of the second charge donor layer and a third portion of said second charge donor layer disposed adjacent said dopant sheet being ~~a relatively lightly doped~~ an undoped region of said first Group III-V material.

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11. The transistor, as recited in claim 10, wherein said first charge donor layer has a first portion adjacent said channel being of an undoped first Group III-V material, 14 an intermediate portion of said charge donor layer adjacent said undoped portion comprised of a dopant sheet of n-type dopant having a concentration of dopant atoms confined to a few atomic layer thicknesses of the first charge donor layer, and a third portion of said first charge donor layer being a relatively lightly doped region of said first charge donor layer with said third portion corresponding to the first charge screen layer.

10 7
12. The transistor, as recited in claim 9, wherein said second charge screen layer is comprised of doped third Group III-V material disposed adjacent the gate electrode and source 14 and drain electrodes of the high electron mobility transistor and having a dopant concentration in the range of about $1X10^{17}$ to $5X10^{17}$ atoms/cc.

11 10
13. The transistor, as recited in claim 12, wherein said first charge screen layer has a first recess having a first width disposed therethrough and a second recess aligned over the first recess having a second, substantially larger width than that of the first recess and disposed

through a portion of the thickness of the second charge screen layer.

14. A high electron mobility transistor comprising:

a substrate;

a channel layer comprised of a first Group III-V material disposed over said substrate;

a charge donor layer disposed over said channel layer comprised of:

a first region of undoped second Group III-V material having a bandgap higher than the corresponding bandgap of the material of the channel layer;

a second region of said charge donor layer having a dopant confined to a few angstroms thickness of said charge donor layer and having a dopant concentration in the range of about $2X10^{12}$ to $5X10^{12}$ atoms per square centimeter; and

a third region comprised of a relatively lightly doped portion of said second Group III-V material compared to the dopant concentration of said second region;

a charge screen layer comprised of a third Group III-V material disposed over said third region of said charge donor layer with said charge screen layer having a portion of lightly doped n-type material;

a gate electrode disposed in Schottky barrier contact with said third ~~portion~~ region of said charge donor layer in a region of said charge donor layer underlying the portion of said charge screen layer which is lightly doped n-type; and

a pair of source and drain electrodes disposed in ohmic contact over said charge screen layer.

~~15~~ 12. The transistor, as recited in Claim ~~13~~ 14, further comprising a pair of spaced contact regions comprised of said ~~first~~ third Group III-V material having a dopant concentration greater than about $1X10^{18}$ atoms per square centimeter disposed between said corresponding pair of source and drain electrodes and said charge screen layer.

16. The structure, as recited in ~~Claim 14~~ Claim 15, wherein said charge donor layer is comprised of aluminum gallium arsenide and said channel layer is comprised of gallium arsenide.

17. The structure, as recited in ~~Claim 14~~ Claim 15, wherein said first material is indium gallium arsenide, said second material is aluminum gallium arsenide, and said third material is gallium arsenide.